REMARKS

The following is intended as a full and complete response to the Office Action dated April 8, 2009, having a shortened statutory period for response set to expire on July 8, 2009. The Examiner provisionally rejected claims 1-5, 7, 10-14, 16, 22-23, 25, 31-35 and 38-40 under the judicially created doctrine of obviousness-type double patenting. The Examiner rejected claims 10-17, 19-24, 31-37 and 38-40 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the inventive subject matter. The Examiner rejected claims 1-4, 7, 10-17, 19-23, 25-27, 29-31, 34 and 38-40 under 35 U.S.C. § 103(a) as being unpatentable over Van Hook (U.S. Patent No. 6,342,892) in view of Bishop (SPARTA: Simulation of Physics on a Real-Time Architecture) and Dakhil (U.S. Patent No. 6,341,318).

Rejections under Double Patenting

The Examiner provisionally rejected claims 1-5, 7, 10-14, 16, 22-23, 25, 31-35 and 38-40 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 2, 5, 7-8, 15, 20, 23, 27, and 30 of co-pending Application No. 10/715,370 and claims 2, 8, and 19 of co-pending Application No. 10/715,440. Applicants acknowledge the double patenting rejection made in the Office Action and respectfully request that the rejection be held in abeyance until the pending claims are in condition for allowance. At such time, an appropriate terminal disclaimer will be filed, if still necessary.

Rejections under 35 U.S.C. §112

The Examiner rejected claims 10-17, 19-24, 31-37 and 38-40 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the inventive subject matter. Specifically, the Examiner rejected claims 10-17 and 19-24 for being dependent of cancelled claims. Applicants have amended claims 10, 14 and 19 and submit that none of the claims is now dependent on a cancelled claim. Therefore, Applicants request the withdrawal of the §112 rejection of claims 10-17 and 19-24.

With respect to claims 38-40, the Examiner rejected those claims for reciting the limitations of the "PPU of claim 1," the "PPU of claim 25," and the "PPU of claim

31," respectively, while the independent claims upon which claims 38-40 depend on recite the limitations of the "system," the "gaming system," and the "personal computer," respectively. Applicants have amended claims 38-40 to recite the limitations of the "system of claim 1," the "gaming system of claim 25," and the "PC of claim 31," respectively. Therefore, Applicants request the withdrawal of the §112 rejection of claims 38-40.

Rejections under 35 U.S.C. §103(a)

Claim 1 recites the limitations of a PPU that comprises a PCE configured to receive physics simulation requests from a CPU via a PPU software driver executing on the CPU and to issue commands to a DME and an FPE to perform physics simulation computations associated with the physics simulation requests. None of the cited references teaches or suggests these limitations.

Van Hook discloses a video game system having a central processing unit (CPU) and a coprocessor that produces audio and video signals. The coprocessor in Van Hook includes a CPU interface and a signal processor. The CPU interface is a gateway for communication between the signal processor and the CPU. The CPU reads from and writes to registers within the CPU interface to control the operation of the signal processor (see Van Hook, column 17, lines 51-54). The signal processor in Van Hook executes audio and graphics tasks based on the register values stored in the registers within the CPU interface (see Van Hook, column 15, lines 30-32 and Figure 6A).

In the Office Action, the Examiner cites the CPU interface for teaching the recited limitations of a PCE configured to receive physics simulation requests from the CPU via a PPU software driver executing on the CPU. However, the disclosed CPU interface is simply a hardware component within the coprocessor that allows the CPU to control audio and graphics tasks executing on the signal processor by reading from and writing to registers. Van Hook does not mention that the CPU interface communicates with the CPU via a PPU driver, or any equivalent thereof.

The Examiner then cites the signal processor for teaching the limitations of a PCE configured to issue commands to a DME and an FPE to perform physics simulation computations associated with the physics simulation requests, as also

recited in claim 1. Applicants disagree with the Examiner's comparison for two reasons.

First, the Examiner argues that because the signal processor includes an execution unit that outputs control signals to other components within the signal processor, the signal processor issues commands to a DME and an FPE, as recited in claim 1. While the execution unit may output control signals to the DMA controller (arguably equivalent to the recited DME), Van Hook does not mention or suggest that the execution unit outputs control signals to the display processor (not within the signal processor) which, in the Office Action, the Examiner equates to the recited FPE.

Second, claim 1 recites a specific architecture including a single system element, i.e., the PCE, that is configured to perform two operations, i.e., receive physics simulation requests from the CPU and issue commands to both the DME and the FPE. The Examiner, however, cites two different system components in Van Hook, the CPU interface and the signal processor, to teach functionality equivalent to the functionality as that of the PCE. The disclosed architecture, shown in Figure 6A of Van Hook, does not include any component that is configured to perform both of the operations recited for the claimed PCE.

Bishop discloses an application-specific integrated circuit that can accelerate physics modeling in conjunction with a CPU. The Examiner relies on Bishop only to demonstrate a Physics Processing Unit (PPU). Thus, Bishop fails to cure the deficiencies of Van Hook.

The remaining references, Intel, Dakhil, Shiell, and Telekinesys, fail to cure the deficiencies of Van Hook and Bishop set forth above with respect to claim 1.

As the foregoing illustrates, no combination of the cited references teaches or suggests each and every limitation of amended claim 1. Therefore, the combination of these references cannot render obvious claim 1, or claims 2-4, 6-9, 18-19, and 22-23, dependent thereon. For this reason, Applicants submit that claims 1 and claim 2-5, 7, 10-17 and 19-24 are in condition for allowance.

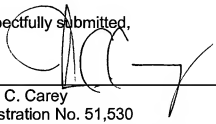
Claims 25 and 31 recite limitations similar to those recited in claim 1 and are, therefore, allowable for at least the same reasons as allowable claim 1. The

remaining claims depend from either allowable claim 25 or 31 and, therefore, are also in condition for allowance.

CONCLUSION

Based on the above remarks, Applicants believe that he has overcome all of the objections and rejections set forth in the Office Action mailed April 9, 2009 and that the pending claims are in condition for allowance. If the Examiner has any questions, please contact the Applicants' undersigned representative at the number provided below.

Respectfully submitted,



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